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Notice of Allowability	Application No. 09/430,350	Applicant(s) SUTERA ET AL.	
	Examiner Hugh Jones	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/9/2004*.

2. ☒ The allowed claim(s) is/are *1-8,14-17,25,27-30,36-39 and 47*.

3. ☒ The drawings filed on ~~6/5/02~~ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

1. Claims 1-8, 14-17, 25, 27-30, 36-39, 47 of U.S. Application 09/430,350 are pending.

Allowable Subject Matter

2. Claims 1-8, 14-17, 25, 27-30, 36-39, 47 are allowed over the prior art of record. The application being allowed, formal drawings are required.

3. The following is an examiner's statement of reasons for allowance: The prior art discloses the following:

- Petschauer et al. ('506) disclose "*Method of fabricating IC chips with equation estimated peak crosstalk voltages being less than noise margin.*" They further disclose that in one method according to the present invention, an integrated circuit chip is fabricated by the following steps:

1) providing a trial layout in the chip for a victim net and a set of aggressor nets which have segments that lie next to the victim net;

2) assigning to the trial layout of the victim net, the parameters of--a line capacitance, a line resistance, and a driver output resistance; and assigning to the trial layout of each aggressor net, the parameters of--a coupling capacitance to the victim net, and a voltage transition;

3) estimating, for each aggressor net, a respective peak crosstalk voltage V.sub.p which the aggressor net couples into the victim net as a function V.sub.p =K(e.sup.-X -e.sup.-Y) where K, X, and Y are products of said parameters;

4) modifying said trial layout and repeating the assigning and estimating steps until a summation of the estimated peak crosstalk voltages in the victim net is within an acceptable level; and,

5) building the chip with the modified layout for which the summation is within the acceptable level. See fig. 4-9, 25 and corresponding text.

- Li et al. (A repeater optimization methodology for deep sub-micron high-performance processors. - 1997)disclose that as process technology scales down to deep sub-micron and the frequency of a high-performance processor increases beyond 300 MHz, coupling induced signal integrity problems become more severe. Ignoring coupling effects can lead to functional failures or speed degradation. As a result, the traditional approach of **repeater** insertion driven by propagation **delay** and slew rate optimization becomes inadequate. The authors propose a design methodology to select optimal **repeaters** for high-performance processors by considering not only the **delay** and slew rate, but also **crosstalk** effects. A concurrent decision diagram (CDD) is further suggested to achieve **crosstalk** constraints with various trade-offs. See section IV (Proposed Methodology) including step 1 (Delay-ratio consideration); step 2 (Repeater-delay consideration); step 4 (With vs. witout repeaters: delay and skew); step 5 (Crosstalk consideration); step 6 (CDD alternatives and trade-offs). Particularly note fig. 3 (crosstalk voltage dependence on wire length); fig. 6 (design algorithm taking into consideration delay, crosstalk wire length, driver strength in an iterative constraint methodology); fig. 11 (delay dependence on presence of repeaters and as a function of

wire length); fig. 13-14 (relationship between crosstalk and driver strength); fig. 15 (relationship between crosstalk, wire length and driver strength).

- ***Alpert et al. ('182)*** disclose a method for ***optimal insertion of buffers into an integrated circuit design***. A model representative of a plurality of circuits is created where each circuit has a receiving node coupled to a conductor and a source. A receiving node is selected from the modeled plurality of circuits and circuit noise is calculated for the selected receiving node utilizing the circuit model. ***If the calculated circuit noise exceeds an acceptable value an optimum distance is computed from the receiving node on the conductor for buffer insertion. See "noise slack"*** at col. 11, for example as it relates to the recited "curves". In a multi-sink circuit merging of the noise calculation for the two receiving circuits must be accomplished. ***If an intersection of conductors exists between the receiving node and the optimum distance a set of candidate buffer locations is generated. The method then prunes inferior solutions to provide an optimal insertion of buffers***. See fig. 3-6. See entire disclosure.

- **Tawada** discloses a system for automatically improving and removing the crosstalk error for reducing the number of designing steps, the switching timing of each net is detected from the results of path delay analysis and crosstalk analysis is carried out so as to take account of the overlap of the switching timing between a net under inspection and a neighboring net. A delay gate insertion unit inserts a delay gate to a neighboring net having timing overlap with the net under inspection undergoing crosstalk error as detected or a net on a path to which belongs the neighboring net. The

delay gate inserted is such a delay gate as can improve the crosstalk and as does not produce path delay error. The delay gate inserted by the delay gate placing unit is placed on the route of the net at such a position as can improve the crosstalk error of the net under inspection. An incremental wiring unit re-wires a net divided by the insertion and placing of the delay gate and a net affected by the insertion and placing of the delay gate to improve the crosstalk error automatically. See fig. 1, 4-5, 9, 14-19 and corresponding text.

- **Jones et al**. disclose ***automated cost-based placement*** (wherein ***cost*** includes timing and ***noise***) of library cells (including buffers) and the use of Design Rule checking (DRC). See: abstract; fig. 1-3, fig. 4 (cell library and speed paths), fig. 5 (timing); col. 1-2 (general background); col. 3, lines 29-65 (details about the placement, cost function, cell library, speed, ***noise***); col. 5, lines 47-60 (cell library, buffers); col. 6, lines 36-47 (goals of optimized placement); col. 7, lines 3-43 (cost and iteration); col. 8, lines 9-42 (***goals of optimized placement***); col. 9-10 (automated, iterative, cost-based layout; timing, ***noise***; DRC). ***Jones et al. teaches noise avoidance as one of many criteria for optimal cell placement.***

- ***Dwyer et al.*** disclose a method (and a system for using the method) for ***placing a semiconductor circuit device between a driver and one or more receivers on the floor space of a chip***. The method includes the steps of: determining respective distances between the driver and each of the one or more receivers; determining a shortest of the distances; determining midpoint along the shortest distance; determining whether the midpoint is predesignated to the floor space of one or

more blocking semiconductor circuit devices; ***placing the repeater at the midpoint if the midpoint is not predesignated to the one or more blocking semiconductor circuit devices; and applying a backoff algorithm to incrementally back away from the midpoint to an optimal location, and placing the repeater at the optimal location, if the midpoint is predesignated to the one or more blocking semiconductor circuit devices.*** The method can also include the steps of: determining whether the to be placed semiconductor circuit device can be placed at a set of incremental locations located along one or more axes away from the midpoint; and placing the to be placed semiconductor circuit device at one of the one or more acceptable incremental locations. The step of determining the set of incremental locations can be performed in a spiral pattern away from the midpoint. ***The semiconductor circuit device to be placed can be, for example, a repeater along the path of a net (length of wire) to regenerate a propagated signal***.

- Oh et al. disclose "*A scaling scheme and optimization methodology for deep sub-micron interconnect.*" They further disclose the requirements for interconnect in deep-submicron technologies and identify critical factors that will require innovations in process technology, process integration and circuit-and-system design techniques. They also describe a scaling scheme for global lines to optimize the interconnect for a given application domain such as microprocessors, ASIC's or memory. For local interconnect they demonstrate that cross-talk is the major challenge which can be addressed by selectively using larger drivers to reduce cross-talk noise when necessary. An interconnect system optimization methodology is also presented that can

be used to determine the geometry parameters of a multi-level interconnect system based on the criterion for performance and reliability. See pp. 321-322, fig. 2-4, 13-14.

- ***Davis et al.*** disclose "*Length, scaling, and material dependence of crosstalk between distributed RC interconnects.*" They further disclose that new general expressions for the transient response time and peak crosstalk of coupled distributed RC interconnects driven by a voltage source with finite rise-time and source impedance are presented. New compact expressions for peak crosstalk voltage reveal a previously unrecognized strong dependence of crosstalk on interconnect length, scaling, driver impedance, and materials properties for typical rise-time dominant interconnect circuits. See pg. 228, fig. 3-5.

- ***Yang et al.*** disclose "*Deep submicron on-chip crosstalk [and ANN prediction]*". They further disclose the effect of crosstalk using three deep submicron technologies. They start the experiment by comparing the different technologies. Then they concentrate on 0.18 /spl mu/m technology to examine the effect of different parameters on the crosstalk voltage peak and circuit timing. The parameters of interest are the size of the driving and load device and the length of the coupled line. The results confirmed that finer technologies cause higher impact. The magnitude of crosstalk in 0.18 /spl mu/m may be high enough to violate noise margin. Preliminary layout guidelines are deduced. To facilitate applying them to CAD tools, an ANN was used to predict crosstalk given data on the driver, the load and the length of the interconnect. See sections 2.2-4.1.

There are two techniques in this art to solve the crosstalk noise problem (which, by definition, inherently depends upon a criterion which defines acceptable vs. unacceptable noise) - 1) increase the driver strength and 2) insert buffers when the conductors are too long. Both were extremely well known in the art at the time of the invention. Applicants have admitted (first paragraph, page 2) that it was known to "*...increase the size of the driver supplying signals to a conductive path which is deemed to be noise sensitive.*". Applicants have also admitted (first full paragraph, page 5) that "*It is well known that a conductive path of a given length being driven by a weak driver will have a higher susceptibility to noise than that same conductive path when driven by a stronger driver.*" Page 6, (second paragraph - lines 1-4) is Applicant's Admission regarding prior art teaching of criterion for noise levels. These features are also disclosed in Oh et al., Davis et al., Yang et al. and Petschauer et al., as noted earlier. If increasing the driver strength is not sufficient to solve the noise problem, then buffers would *also* be required to reduce the noise. Furthermore, If the placement of buffers is not sufficient to solve the noise problem, then increasing the strength of the drivers would *also* be required to reduce the noise.

However, The prior art of record, while disclosing the above mentioned features, does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this

*is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."*

4. In particular, the "examining" and "modifying" (as defined in the specification and recited in the last two limitations of claim 1, for example) are not expressly disclosed in the art in the same manner, in the context of the claims. The claims are thus novel and non-obvious over the prior art of record. Therefore, the art of record does not read on the claims and the claims do not read on the art of record.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to:

Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)
or (703) 308-1396 (for informal or draft communications, please label "*PROPOSED*"
or "*DRAFT*").

Dr. Hugh Jones

Primary Patent Examiner

July 22, 2004

HUGH JONES PH.D.
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TECHNOLOGY CENTER 2100